December, 1982 MRDC41070.18OR

LSI/VLSI ION IMPLANTED GaAs IC PROCESSING

Quarterly Technical Report No. 6

For Period 11/01/81 through 01/31/82

Contract No. F49620-80-C-0101

Project No. 3384-4

ROCKWELL INTERNATIONAL
Microelectronics Research and Development Center
Thousand Oaks, CA 91360

Sponsored by:

Advanced Research Projects Agency (DOD)

ARPA Order No. 3384-4

Monitored by AFOSR under Contract No. F49620-80-C-0101

Prepared by:

Ricardo Zucca
R. Zucca
Principal Investigator

A. Firstenberg
Principal Investigator

Rockwell International

UNCLASSIFIED

SECURITY CLASSIFICATION OF THIS PAGE *(When Data Entered)*

REPORT DOCUMENTATION PAGE	READ INSTRUCTIONS BEFORE COMPLETING FORM
1. REPORT NUMBER: AFOSR-TR- 83-0039	2. GOVT ACCESSION NO.: AD A125 014
	3. RECIPIENT'S CATALOG NUMBER:
4. TITLE *(and Subtitle)*: LSI/VLSI ION IMPLANTED GaAs IC PROCESSING	5. TYPE OF REPORT & PERIOD COVERED: Quarterly Technical Report, 11/01/81 through 01/31/82
	6. PERFORMING ORG. REPORT NUMBER: MRDC41070.18QR
7. AUTHOR(s): R. Zucca, Y. D. Shen, P. Asbeck, C. G. Kirkpatrick, A. Firstenberg	8. CONTRACT OR GRANT NUMBER(s): F49620-80-C-0101
9. PERFORMING ORGANIZATION NAME AND ADDRESS: ROCKWELL INTERNATIONAL/Microelectronics Research and Development Center, 1049 Camino Dos Rios, Thousand Oaks, CA 91360	10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS: ARPA Order No. 3384-04, 6110ZF
11. CONTROLLING OFFICE NAME AND ADDRESS: Advanced Research Projects Agency (DOD), 1400 Wilson Boulevard, Arlington, VA 22209	12. REPORT DATE: December 1982
	13. NUMBER OF PAGES: 32
14. MONITORING AGENCY NAME & ADDRESS *(if different from Controlling Office)*: Air Force Office of Scientific Research, Bolling Air Force Base, Washington, DC 20332	15. SECURITY CLASS. *(of this report)*: UNCLASSIFIED
	15a. DECLASSIFICATION/DOWNGRADING SCHEDULE:

16. DISTRIBUTION STATEMENT *(of this Report)*

Approved for public release; distribution unlimited

17. DISTRIBUTION STATEMENT *(of the abstract entered in Block 20, if different from Report)*

This research was sponsored by the Advanced Research Projects Agency (DOD) ARPA Order No. 3384-4

18. SUPPLEMENTARY NOTES

19. KEY WORDS *(Continue on reverse side if necessary and identify by block number)*

Semi-insulating	High Speed Logic
Ion Implantation	GaAs
IC	FET
Integrated Circuits	MESFET

20. ABSTRACT *(Continue on reverse side if necessary and identify by block number)*

This report covers the sixth quarter of a program aimed at fully realizing the potential of GaAs for digital integrated circuits employing depletion mode MESFETs. During this reporting period, large single crystals of GaAs have been grown by the Bridgman technique of Crystal Specialties. In the area of processing, a study was made of the dependence of threshold voltage on the post-implantation anneal time. This study indicates that the anneal time used in the IC process is adequate. LSI yield test structures consisting of long parallel meander lines were used to evaluate various options for metal depositions. Magnetron sputtering was

DD FORM 1 JAN 73 1473 EDITION OF 1 NOV 65 IS OBSOLETE

UNCLASSIFIED

SECURITY CLASSIFICATION OF THIS PAGE *(When Data Entered)*

the preferred technique. The yield of long chains of interconnects was also evaluated. The 8 x 8 multiplier circuit implemented with SD^2FL gates was tested. Work continued on MESFET modeling. The effects of shortening the source-drain gap were evaluated.

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

LIST OF ILLUSTRATIONS

FOREWORD

The research covered in this report was carried out in a team effort having the Rockwell International Microelectronics Research and Development Center as the prime contractor, with two universities and a crystal manufacturer as subcontractors. The effort was sponsored by the Defense Sciences Office of the Defense Advanced Research Projects Agency. The contract was monitored by the Air Force Office of Scientific Research. The Rockwell program manager was Fred H. Eisen. The principal investigators for each organization were:

Microelectronics Research and Development Center	R. Zucca, A. Firstenberg
California Institute of Technology	M-A. Nicolet
North Carolina State University	N.A. Masnari
Crystal Specialties	W.P. Allred

Numerous other researchers have been involved in the work reported herein. The principal contributors are:

Microelectronics Research and Development Center	P.M. Asbeck, A. Firstenberg W.P. Fleming, G.R. Kaelin, C.G. Kirkpatrick, C.P. Lee, F.S. Lee, S.J. Lee, M.J. Sheets, E.K. Shen, Y.D. Shen, E.R. Walton, J.O. Thompson B.M. Welch, R. Zucca
California Institute of Technology	T. Banwelo, M. Martimaenpaa,
North Carolina State University	J.R. Hauser, T.H. Glisson R.J. Trew
Crystal Specialties	J. Burns

1.0 INTRODUCTION

This report covers the sixth quarter of a program on LSI/VLSI Ion Implanted Planar GaAs IC Processing. The main objective of this program is to realize the full potential of GaAs digital integrated circuits by expanding and improving fabrication techniques as well as material growth, preparation and selection. The principal goal is to improve material and processing capabilities so that large wafers (three inch diameter) can be processed in order to satisfy anticipated needs for high-speed low-power GaAs digital VLSI integrated circuits. In parallel with increasing circuit complexity and wafer size, the program is also directed toward the investigation of circuit reliability, and the development of processing techniques and circuit designs capable of attaining the highest reliability. Circuit design advancements are also explored. Three subcontractors, the California Institute of Technology, North Carolina State University, and Crystal Specialties, Inc. are contributing to the program with their expertise in ion beam techniques, device modeling, and crystal growth, respectively.

While equipment preparation for processing of large wafer has continued, several aspects of process development have received attention. The work in this area is aimed at improving device performance, process yield, and circuit reliability, and it is supported by a sustained effort in semi-insulating substrate analysis and ion implantation development. Circuit testing has been carried out, and modeling activities have continued.

Growth of large single crystals of GaAs has been addressed at Crystal Specialties. Large single crystals have been grown by the Bridgman technique in 1 × 2.5 × 4 inch boats. One hundred wafers oriented in the (100) direction, as large as 2.4 × 4 inches, were cut from these crystals.

Efforts to continue investigating all the factors that can control the reproducibility and uniformity of FET threshold voltages have continued. In this quarter very high uniformity was demonstrated in a study of the variation of threshold voltage, V_p, for wafers sampled along the length of an LEC

ingot of undoped material grown from a PBN crucible. The relative variation of V_p was found lower than the resistivity variation along the ingot.

A study was made of the dependence of the threshold voltage obtained on the post-implant anneal time. Relatively rapid variation of V_p with anneal time was observed below thirty minutes, and slow variation was observed above this time which is the nominal time used in the IC process. This result indicates that the currently used annealing time is adequate.

Progress has continued on evaluating LSI process yield on experimental test structures, in parallel to circuit fabrication. Comparisons of second level metal yield obtained using various E-beam deposition systems and magnetron sputter deposition have been made using a test structure which consists of very long meander lines. The experiments showed that magnetron sputtering is the preferred technique for the multi-level metal application. Yield assessment of long via chains was also completed during this quarter.

The 8 × 8 multiplier circuit implemented with SD^2FL gates was tested. The circuit was not found functional. A thorough investigation of functionality on the lowest order three product bits which involve only a few gates was done on several chips from several wafers with varying bias conditions. Errors were observed in all cases. Since SD^2FL gates did operate properly in previous designs, it is suspected that design and layout changes made with the intention to improve performance may be related to the failure. Since revised performance predictions do not indicate sufficient advantages for the SD^2FL design over a simple SDFL multiplier, effort to further investigate the cause of the failure were not continued.

MESFET modeling work has continued in these directions: two-dimensional modeling; an analytical model; and Monte Carlo calculations. The two-dimensional model was used to compare 1 μm gate MESFETs with 0.5 μm and spacing between the edges of the gate and the source/drain contacts with similar MESFETs having a 0.25 μm gate to source/drain spacing. The short gap devices had a 6.2% higher transconductance, but his advantaage was partly offset by

larger gate capacitances leaving a modest increase of 5% in gain-bandwidth product.

The work on Bridgman growth of large crystals is discussed in Section 2.0. Threshold voltage uniformity is discussed in Section 3.0. The experiments on metallization yield are covered in Section 4.0. In Section 5.0, the results of testing the 8 × 8 bit SD^{2}FL multipliered are discussed, and MESFET modeling is addressed in Section 6.0.

2.0 GROWTH OF LARGE CROSS SECTION GaAs SLICES USING THE HORIZONTAL BRIDGMAN METHOD

Work at Crystal Specialties has resulted in the growth of several large area single crystals of gallium arsenide using the horizontal Bridgman technique. (100) wafers cut from these crystals measured 2.5 inch wide and 4 inches long. The crystals were grown in a quartz boat 1 inch deep, 2.5 inches wide and 4 inches long. The seeds were oriented with the growth direction on the (110) axis so that the (100) axis is in the vertical direction. By cutting the crystal perpendicular to the vertical (100) avis, wafers as large as 2.5 × 4 inches could be produced. Since cutting equipment large enough to slice this large area was not available, the ingot was trimmed to about 2.5 × 3 inches before cutting.

3.0 DEPENDENCE OF FET THRESHOLD VOLTAGE ON MATERIAL AND ON ANNEAL TIME

Uniformity of the GaAs substrate material is an important prerequisite for the reproducibility of implanted device characteristics. The uniformity of Bridgman-grown semi-insulating ingots have already been studied in detail as part of this progrm. In this quarter, studies have been continued on liquid-encapsulated-Czochralski (LEC) grown ingots, to verify their suitability for use in the planned Rockwell 3 inch process line. Very good uniformity across 3 inch wafers of undoped, semi-insulating LEC GaAs grown at Rockwell as part of an IR&D effort has already been described. In this quarter, measurements were made of the uniformity along the length of the LEC ingot. The results, again, showed excellent uniformity. For this study, test chips were cleaved from sample wafers selected along the length of an ingot, and subsequently capped, implanted with Se and annealed together in the standard fashion. The depletion voltages, V_d, obtained for these test chips from C-V measurements are illustrated in Fig. 1. The excellent longitudinal uniformity is apparent in the less than 100 mV variation from front to tail.

The ingot used in the uniformity test corresponds to a worst-case study. In fact, for nearly all Rockwell-grown ingots measured, the bulk resistivity is uniformly high ($> 10^8$ Ω/□) along the ingot length. On several ingots, however, p-conductivity developed towards the tail region. The ingot of Fig. 1 corresponds to such a case, as determined by resistivity measurements of unannealed test chips, whose results are also shown in the figure.

The fact that p-type conductivity occurs in unimplanted material while no doping change occurs in Se-implanted layers is well explained by a compensation model developed as part of Rockwell's IR&D effort. In the unimplanted material, the carrier density is determined by the balance between carbon acceptors (uniformly distributed along the ingot length) and EL2 deep donors, whose concentration decrease along the ingot length because the material became progressively enriched with Ga during crystal groth. In the implanted n-type material, however, the varying EL2 concentration has no

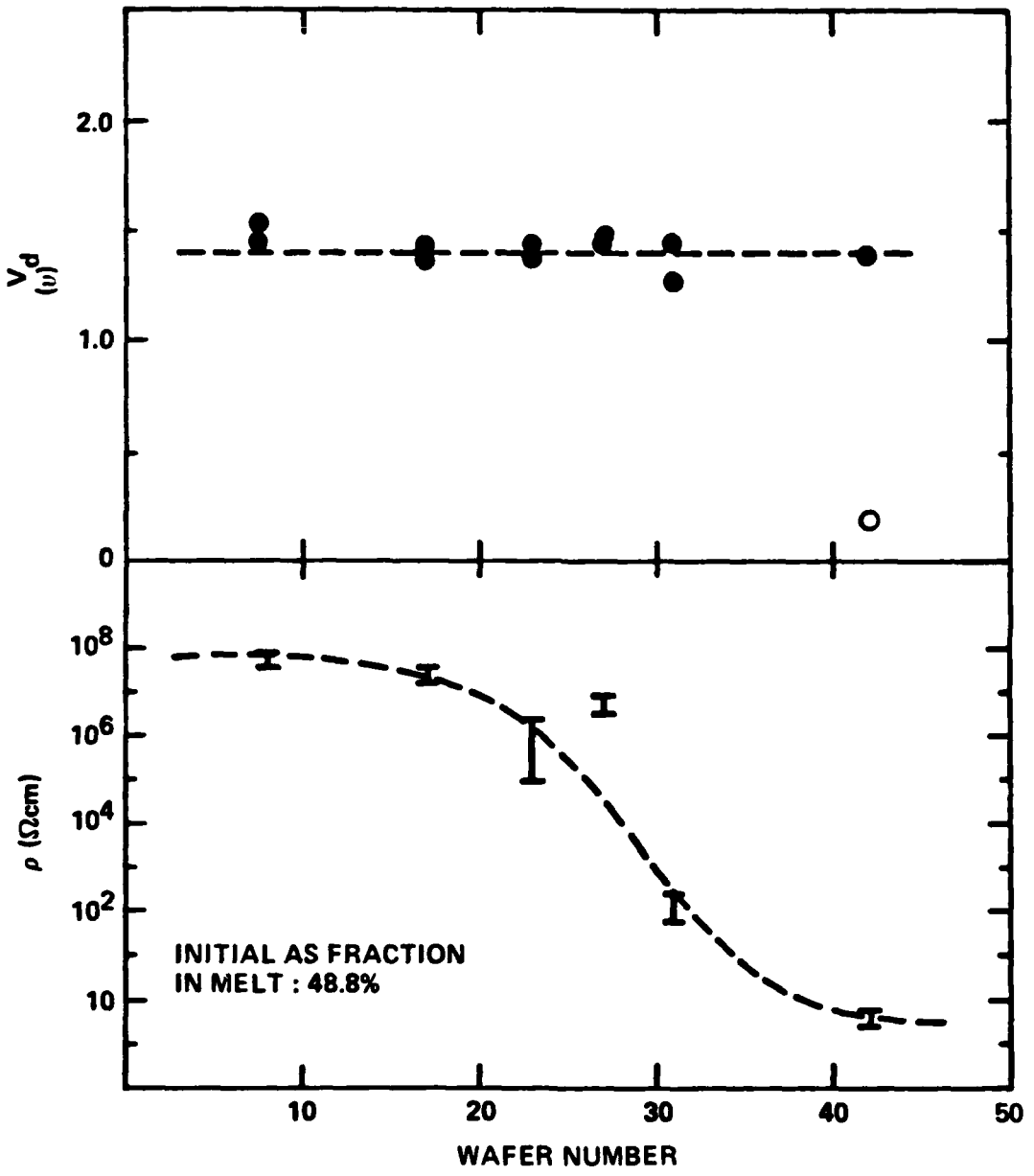


Fig. 1 Variation of the depletion voltage along the length of an LEC ingot. The data correspond to a worst case variation of bulk resistivity along the ingot, as shown by the lower curve.

effect since these deep donors are neutral; the electron density is determined by the balance beteen the (spatially uniform) Se donors and the (spatially uniform) carbon acceptors.

In parallel with studies of the substrate material, further investigation of the effects of implant process variations was carried out. In this quarter variations in the anneal time were studied. Test chips of Cr doped or undoped semi-insulating GaAs were capped, Se-implanted and then annealed for varying periods of time at 850°C. C-V measurements were then done to determine carrier profiles and depletion voltages, V_d. The carrier profiles for long anneal times showed increase depth and lower peak carrier densities compared with the standard 30 minutes as qualitatively expected for Se diffusion.

Significant activation was found for anneals as short as 8 minutes. The variation of V_d with anneal time is shown in Fig. 2. It is apparent that V_d is quite sensitive to the time in the range below 30 minutes, suggesting that the current process represents a good compromise beteen limiting diffusion and avoiding significant V_d variations. No significant difference was found between the behavior of Cr doped and undoped substrates, indicating that the changes in V_d from Cr diffusion occur rapidly (in less than 5 minutes), and then saturate due to Cr depletion, so that further changes are apparently related only to Se diffusion.

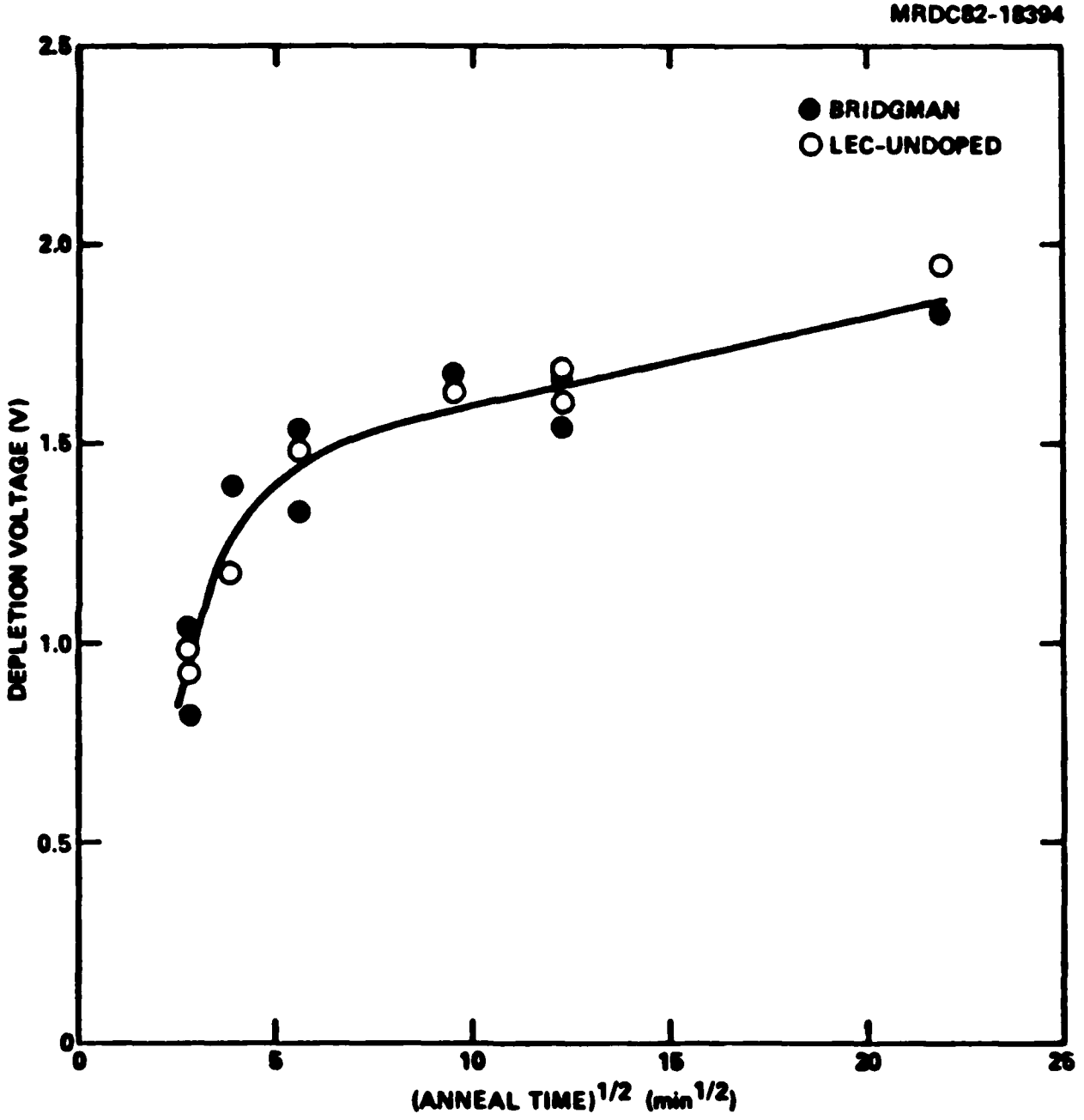


Fig. 2 Depletion voltage of Se implanted wafers (at a dose of 2.5×10^{12} ions/cm^2) as a function of the anneal time. The implants were made in semi-insulating GaAs substrates. The annealing cap consisted of sputtered Si_3N_4.

4.0 METALLIZATION YIELD

In this quarter, efforts were made to further investigate the yield of second level interconnect lines and to determine the yield of interconnects. Both activities are discussed in this section.

4.1 Yield of Second-Level Metal Lines

A yield test mask has been fabricated and used to evaluate the second-level metal process. Results comparing the yield of second level metal deposited by E-bem evaporation vs magnetron sputtering were shown in the Quarterly Technical Report No. 4. The yield of long parallel lines resulting from E-beam evaporation is much lower than the yield resulting from magnetron sputtering because of splattering occurring during evaporation. However, and despite the lower yield, the higher conductivity (1.7 times) of E-beam evaporated Au films over magnetron sputtered films makes E-beam evaporation an attractive technique for second-level metal deposition. Therefore, a more extensive evaluation of E-beam evaporation systems was carried out.

In order to minimize splatter from evaporation, the evaporator used for this process was upgraded so that the E-beam could be swept over the Au source. However, the yields resulting from wafers deposited by this system were still about the same as those described in Report No. 4, while being more reproducible. The data base was also expanded by evaluating wafers on which Au was deposited by two evaporators used for other GaAs programs. It was found that the wafers processed with the standard IC evaporation equipment had better yields. A summary of all the yield data obtained is shown in Fig. 3. The points in the figure represent averages over the following data base:

Magnetron Sputtering - IC Equipment	2 runs, 4 wafers/run
E-Beam Evaporation - IC Equipment	2 runs, 4 wafers/run
E-Beam Evaporation - System A	1 run, 4 wafers/run
E-Beam Evaporation - System B, Run 1	1 run, 2 wafers
E-Beam Evaporation - System B, Run 2	1 run, 2 wafers

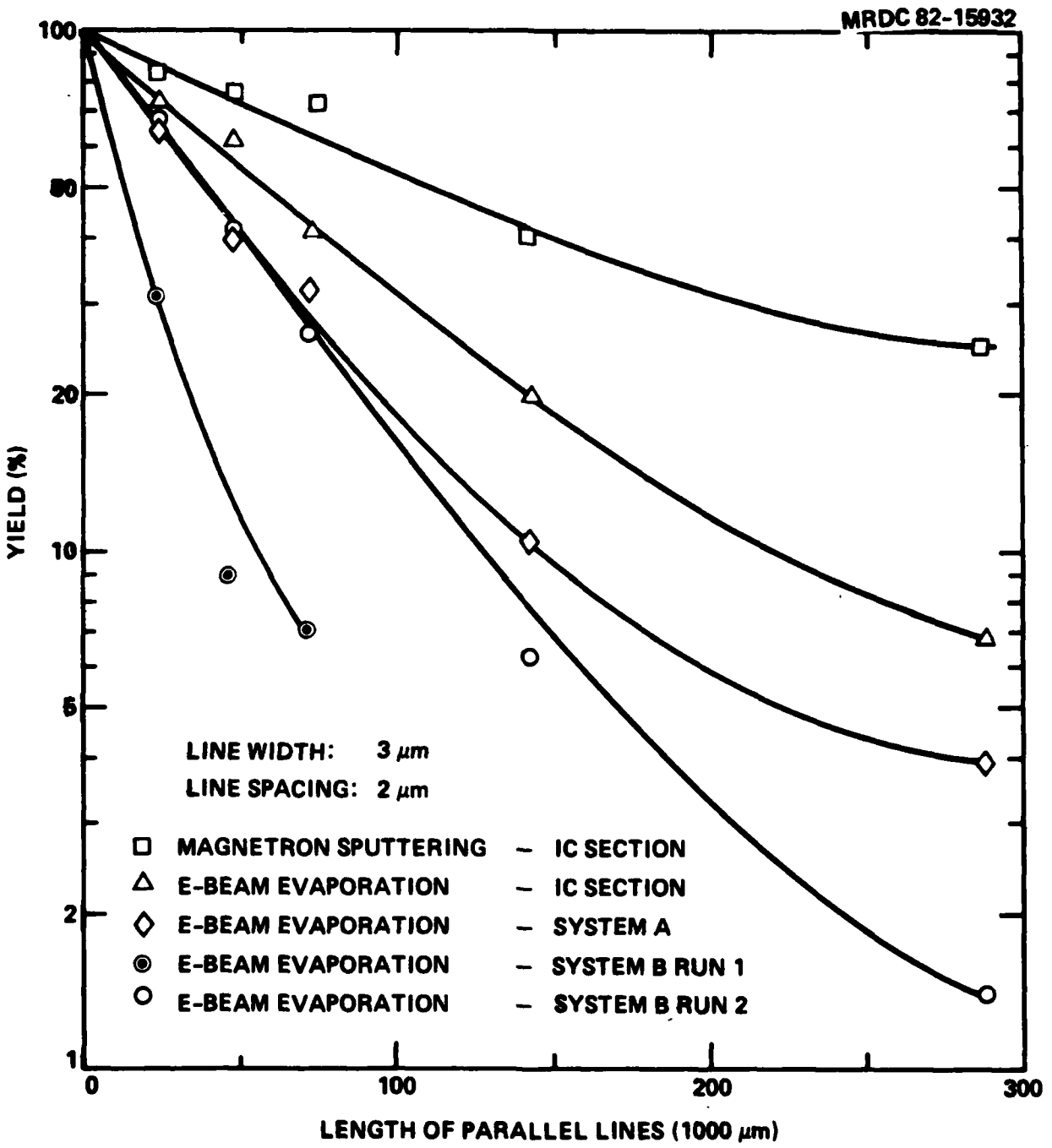


Fig. 3 Yield of parallel second level metal lines fabricated using several different metal deposition systems. The lines were defined by ion milling.

As described in Report No. 4., the test pattern was repeated 72 times on each wafer. The automatic parametric test system used for process monitoring was used to collect the data and provide statistical information.

Run 1 and 2 of System B were done within the same pump-down cycle using the same parameters except that the first run serves as a long soak time for the second run. The photolithography and ion million of all wafers from both run 1 and 2 were done at the same time. The fact that the wafers of run 2 have much higher yield than the wafers of run 1 suggests that a proper soaking of the melt may reduce splattering significantly.

In conclusion, magnetron sputtering remains the preferred metal deposition technique for second level interconnects, and it was adopted as the standard technique in our fabrication line. Although some improvements in specific resistivity are desirable, the current resistivity values are quite acceptable, and they are taken into account in the design.

4.2 Yield of Multi-Level Interconnects

As the complexity and size of the integrated circuits increase, the number of multi-level interconnects and crossovers increases dramatically. Therefore, the integrity and yield of crossover structures and multi-level interconnects is an important factor for successful LSI/VLSI fabrication. The yields of crossover structures were discussed in the Quarterly Technical Report No. 3. Here, the results from the evaluation of the yield of long chains of interconnects, are presented.

The interconnect test structure used in this study consists of a chain of first to second level metal interconnects. A drawing of the cell used to build the long chain is shown in Fig. 4. Alternating short strips of Schottky (first level) metal and second level metal are interconnected through via holes. The typical thicknesses of the Schottky metal and the second level metal are 3000 Å and 6000 Å, respectively. The dielectric which separates the Schottky metal and the second level metal consists of 5000 Å thick plasma deposited Si_3N_4. To save space on the wafers, the interconnect test structure

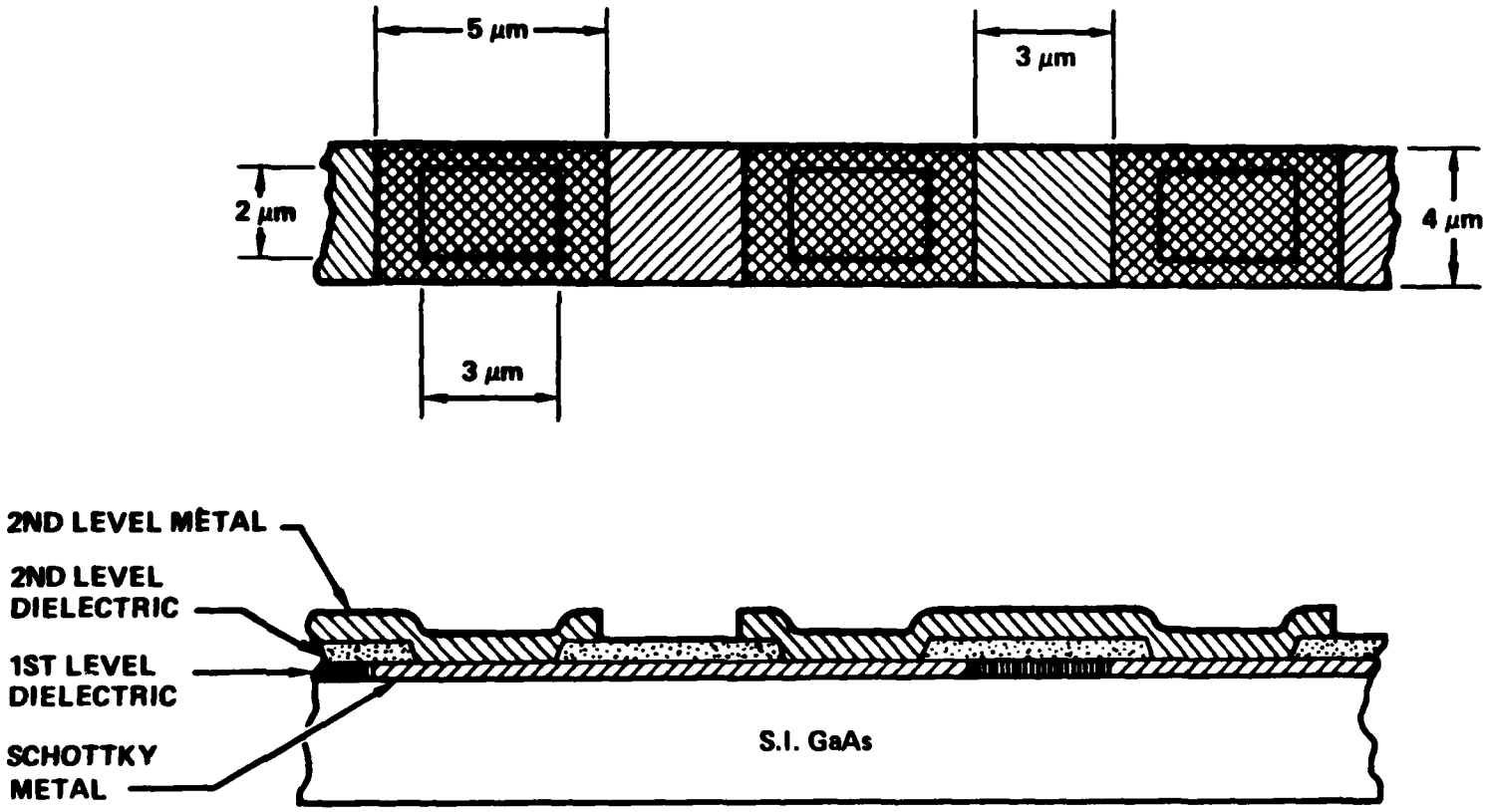


Fig. 4 Schematic of the cell used to build a long chain of first/second level interconnects.

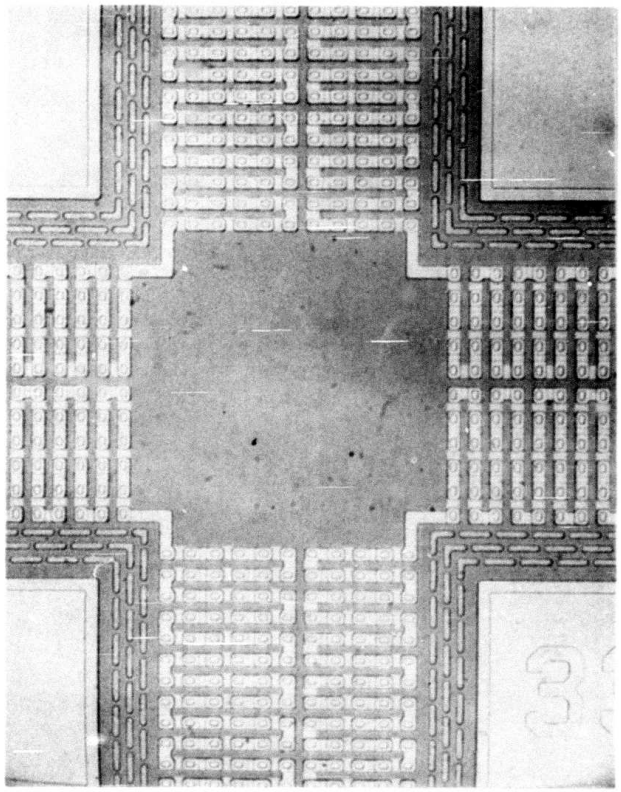
was laid out as a long meander in the kerf lines. A portion of the pattern is shown in Fig. 5. The total length of the pattern includes 14878 interconnects. Note, as a reference, that an 8 × 8 multiplier (1000 gates circuit) has ~ 7000 interconnects.

The integrity of the interconnects was electrically tested by injecting a current of 4 mA through the string. This value was chosen based on our design rule which allows for a current density of 2 mA/μm^2. For a 3000Å thick, 4 μm wide Schottky metal line such as the one used in the interconnect test structure (Fig. 4) the maximum current allowed in a circuit would be 2.4 mA. A 4 mA test current is almost twice the circuit design value. The test can only determine if a string of interconnects is continuous (has current flow) or broken (has no current flow). The test cannot indicate if any elements in the string are shorted together unless a long chain of the string is shorted so that an abnormally low resistance is observed.

The yields obtained are indicated in Fig. 6. They represent the averages obtained from 20 wafers. The yield of 400 interconnects is 100%. It decreases slowly to ~ 65% for the maximum number (14878) of interconnects. The interpolated yield for 7000 interconnects, the number in the 8 × 8 SDFL multiplier, is slightly over 80%. This is a satisfactory number today. However, further improvements will be needed for higher circuit complexity.

The average resistance of each via is 0.077 Ω, which is the same as the resistivity of a square of 3000 Å Au Schottky metal (0.078 Ω/□). This value is low enough because it means that the interconnect resistance is negligible with respect to the line resistance. From a process standpoint, this low value indicates that the surface of the Schottky (first level) metal inside the vias are clean after via window etching, and the second level and first level metal make very good contact. Although not needed at this time, further improvements can be made by filling the vias with metal immediately after etching them. This procedure was successfully demonstrated, but not incorporated into the standard process in order to keep the number of process steps to a minimum.

MRDC81-14303



VIA SIZE: 2 x 3 μm
TOTAL NUMBER OF VIAS: 14,878
VIA RESISTANCE: 0.077Ω/VIA
YIELD: 4,162 VIAS – 83.5% (20 WAFERS TESTED)
14,878 VIAS – 62.5% (20 WAFERS TESTED)

Fig. 5 Portion of the long meander forming the interconnect integrity test structure.

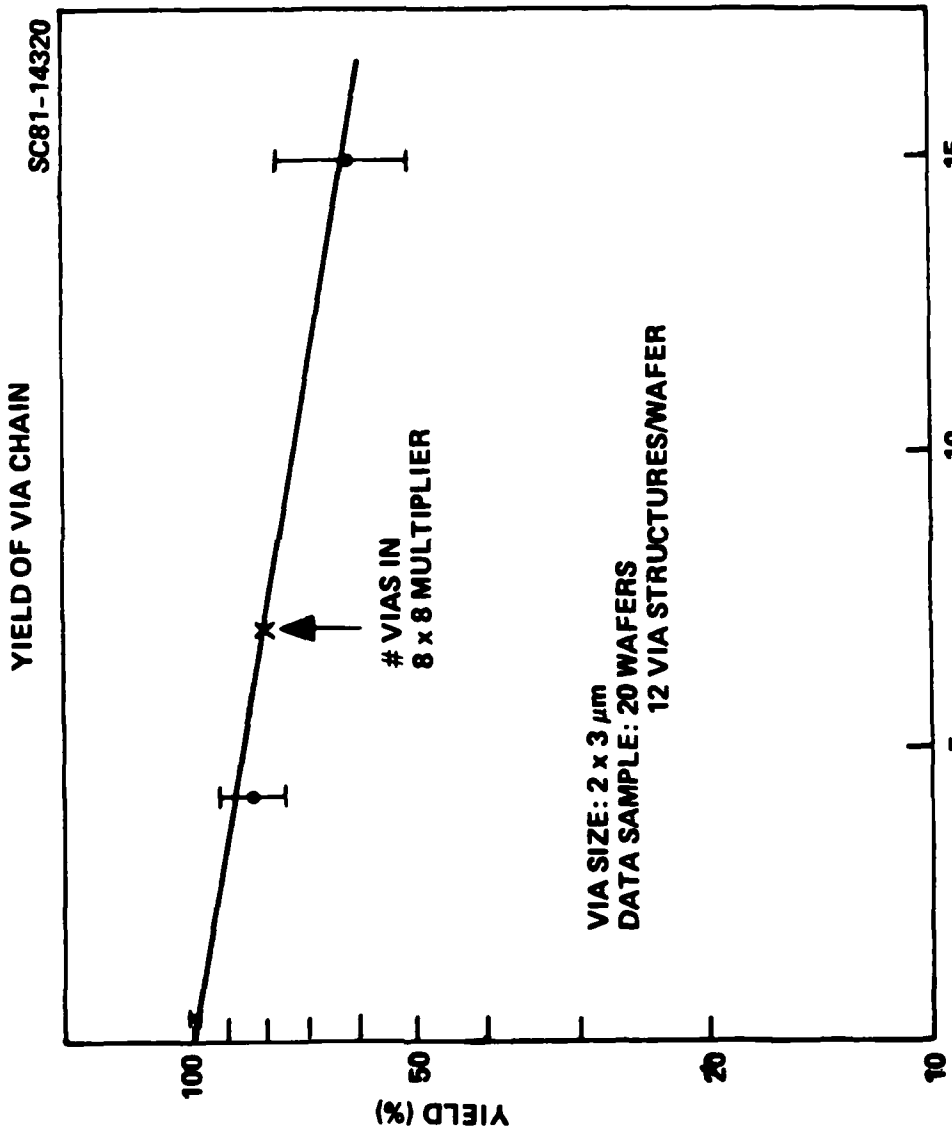


Fig. 6 Yields of first/second level interconnects.

5.0 EVALUATION OF THE SD^{2}FL 8 × 8 MULTIPLIER CIRCUIT

SDFL (Schottky Diode FET Logic) gates can be used to perform multilevel functions such as OR-NAND. However, the number of AND terms is practically limited to two because the AND operation is performed by a multiple gate FET. More than two gates cause the device series resistance to become too high. An extension of the SDFL gate which allows for AND/NOR operations with an almost unlimited number of terms is the SD^{2}FL (Schottky Diode-Diode FET Logic) gate, shown in Fig. 7. This gate type does not impose any severe limitation to the number of AND terms because the AND operation (as well as the OR operation) is performed by diodes.

The ample flexibility of the SD^{2}FL gate makes it quite suitable for certain logic functions, such as multiplexing, where propagations delay as well as power dissipation and chip area can be saved due to its multilevel capability. In order to test the SD^{2}FL gate experimentally on a large circuit, a new version of the 8 × 8 parallel multipler which had been successfully implemented with SDFL gates was incorporated on mask set AR6. On hindsight, this was not a fair test for SD^{2}FL. As discussed in the Quarterly Technical Report No. 2, an array multiplier benefits less than almost any other circuit from a SD^{2}FL implementation. The reason is that both true and complement values of the sum and carry outputs of each adder must be generated and routed as interconnections. This increases both the gate count and the routing area. Power dissipation tends to be high because two of the four gates that generate the sum and carry and their complement must always be on. In summary, the size of a SD^{2}FL full adder is approximately 90% of that of a SDFL adder. The averge power dissipation as expected to be 90% higher than that of a SDFL adder, for a predicted 70% increase in speed.

The multiplier designed on mask set AR6 consists of an 8 bit × 8 bit array of SD^{2}FL adders, and latch circuits for inputs and outputs implemented with conventional SDFL gates. The full 8 × 8 multiplier is a very complex and large chip, which has the following impact on testing. First, the bias

ERC80-8777

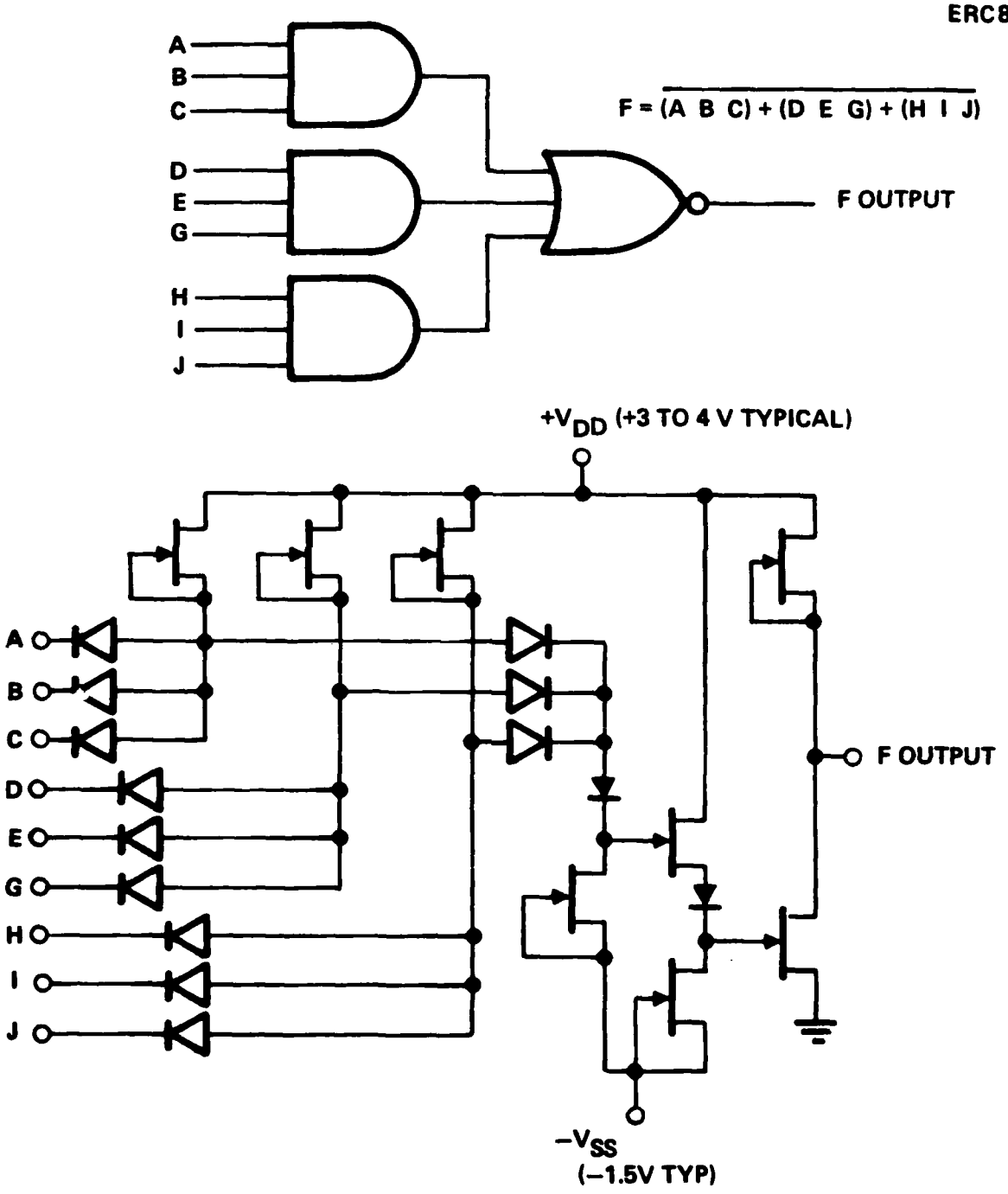


Fig. 7 Schematic of a Schottky Diode-Diode FET Logic (SD^2FL) gate.

sensitivities of the two types of gates (SD^2FL and SDFL) are expected to be slightly different. Secondly, the yield on such large chips is anticipated to be low enough that a considerable number of chips would need to be tested to find fully functional ones. This testing would be made more difficult by the uncertainty of proper bias voltage conditions.

To overcome these potential testing limitations, the multiplier was designed with an alternate second metal mask that eliminated the latches, and subdivided the array into four smaller arrays (two 4 × 4 and two 3 × 4 arrays). This alternate connection layer would be used on the first lots of wafers to facilitate testing on the smaller SD^2FL arrays, which should have higher yield of working arrays, with outputs directly measurable so that bias voltage effects could be observed. Later lots would be processed with the fully connected mask layer.

Testing was started by checking a few circuits for functionality, using a ripple test, while adjusting voltages. From these, a number were identified that had no shorts, showed some degree of functionality, and exhibited output waveforms with well defined voltage levels. These were then tested in more detail, using the lower order bits in the upper right-hand corner. In Fig. 8 a functional diagram of the upper right corner, and the elements involved are shown. Specifically, the gate that combines a_0 and b_0 to form the LSB of the product, P_0 is a SDFL gate, so that SDFL performance can be evaluated. The gates and adders that form P_1 and P_2 are completely SD^2FL. The number of data paths is limited, so that correct operation can be verified; there are 32 unique combinations for this adder circuit. Unfortunately, under testing, it was found that lack of access to circuit nodes make it difficult to ientify specific faults. For example, P_1 is the sum output of a single field adder; its operation can be verified for the sum, but not for the carry. Similarly, the other adders are not fully accessible.

The adder corner combination was tested on several chips, for all input combinations, with varying bias conditions. The chips tested were selected for well defined output levels. None of the chips functioned

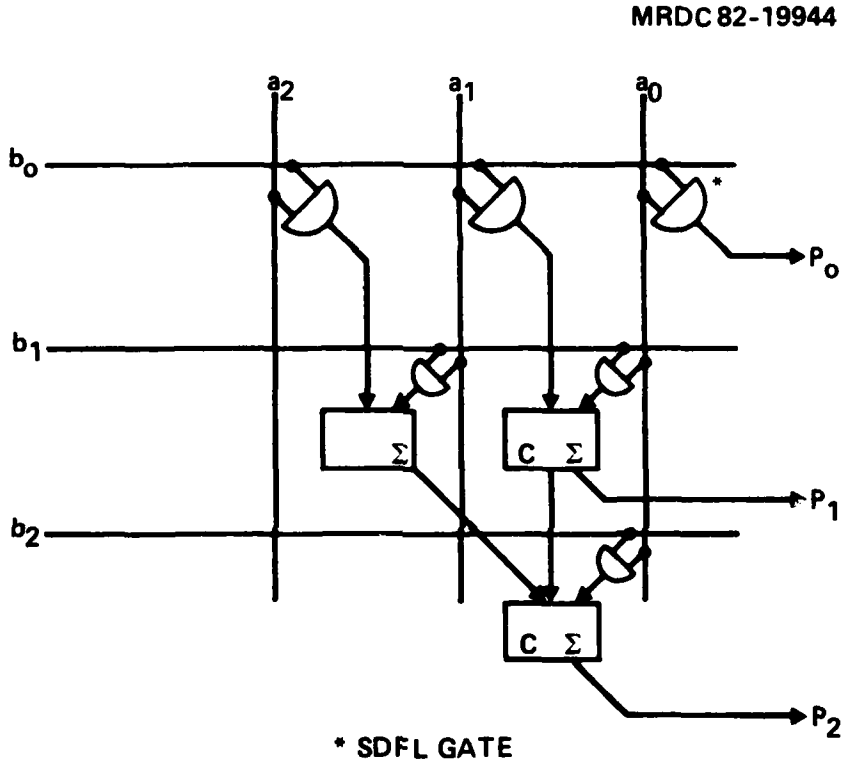


Fig. 8 Schematic of upper right corner (low order bits) of the SD^2FL multiplier.

completely. The failure were not consistent between input combinations; in some cases, for example, several combinations would produce an erroneous output only if a single gate had failed, but several other combinations would produce outputs that required that same gate to function. The testing was carried out to the point where it was suspected that voltage variations within the circuit during operation were affecting operation of some gates.

Testing of SD^2FL gates on previous mask sets has shown that the SD^2FL gate can operate as designed. The testing on AR6 has shown that an SD^2FL adder also operates. It is evident that cascading them results in interactions that have not been considered in the design. It is suspected that design and layout changes made with the intention to improve performance may be related to the failures.

Since the revised performance predictions discussed in Report No. 2 do not indicate sufficient advantages for the SD^2FL design over a simple sDFL multiplier, efforts to further investigate the cause of the failure were not continued.

6.0 MESFET MODELING

During this quarter, efforts have continued in three aspects of MESFET modeling at North Carolina State University.

6.1 Two-Dimensional Numerical Modeling of FETs

In view of the circuit speed improvements observed at Rockwell on circuits in which the FET source-drain separation was tightened, a comparison was made of two ion implanted FET structures. One was a standard geometry device with a 1 μm gate length and 0.5 μm spacing between the gate and the source or drain contacts. The other device had the same 1 μm gate length but had a 0.25 μm spacing between the gate and the source or drain contacts. For comparison purposes, these are labeled as the 0.5 μm and 0.25 μm devices. This notation is not to be confused with the gate length which was 1 μm in both devices.

Figures 9 and 10 show a comparison of the electron densities in the two devices for zero applied gate voltage, and a drain voltage of 2.5 V. As can be seen in Fig. 10, the carriers for the 0.25 μm spacing are depleted all the way up to the contact on the drain side of the gate, as opposed to the 0.5 μm spacing where the depletion region does not extend completely to the drain.

In considering the comparison of devices with 0.5 μm and 0.25 μm spacings one would expect a larger f_m for the 0.25 μm spacing because of the reduction in source-to-gate and gate-to-drain resistance. This would tend to increase f_τ, and consequently, the switching speed for the 0.25 μm spacing. However, for the case shown in Fig. 10 where the depletion region extends completely to the drain contact, one would also expect an increase in the gate-to-drain capacitance for the 0.25 μm device. This would tend to decrease f_τ and the switching speed.

Table 1 shows a comparison of f_τ and other small-signal parameters of the two devices operating at 2.5 V drain bias. The calculations agree with

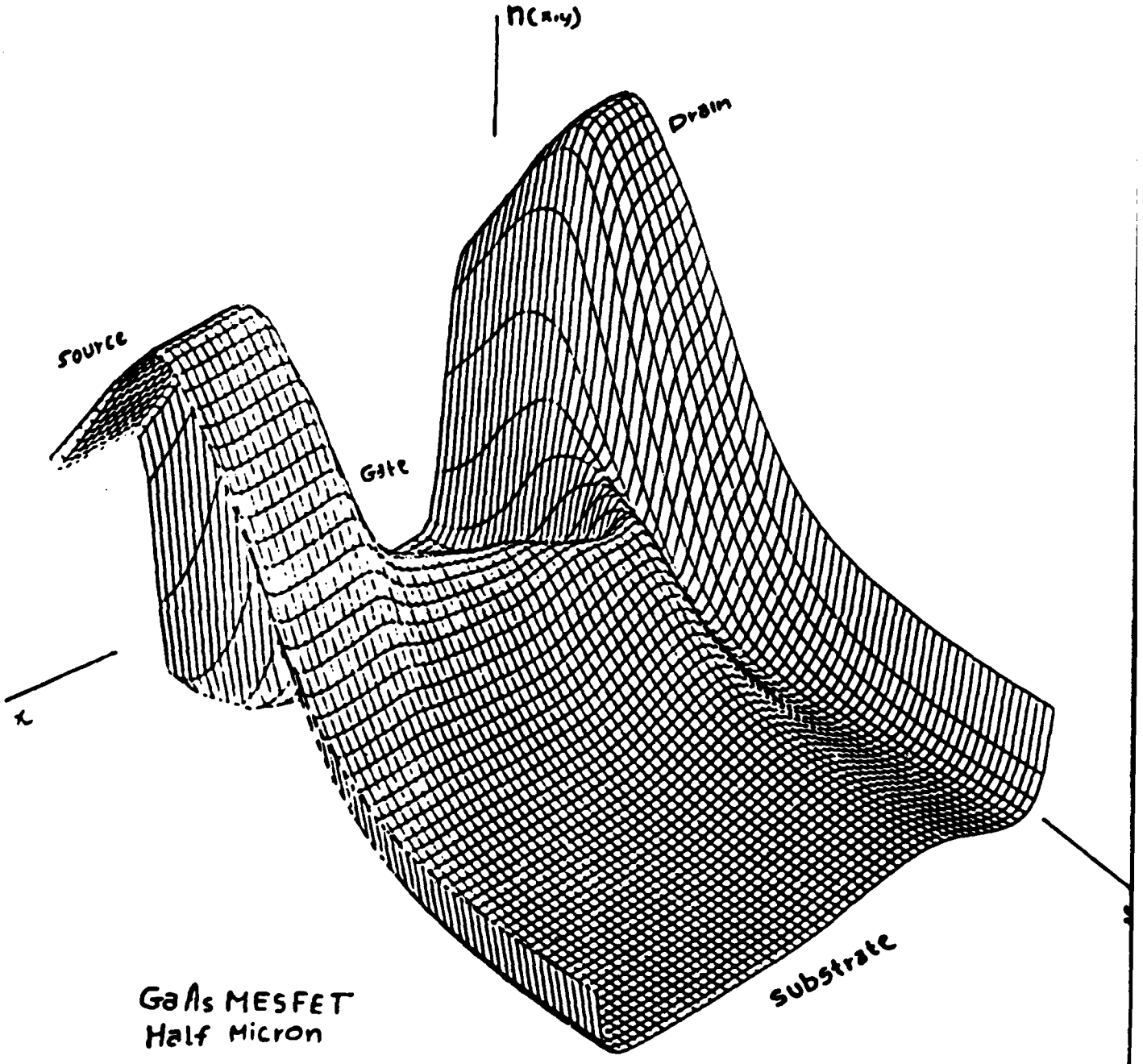


Fig. 9 Electron concentration for a 1 μm gate MESFET with 0.5 μm spacing between the gate and the source/drain contacts at V_{ds} = 2.5 V.

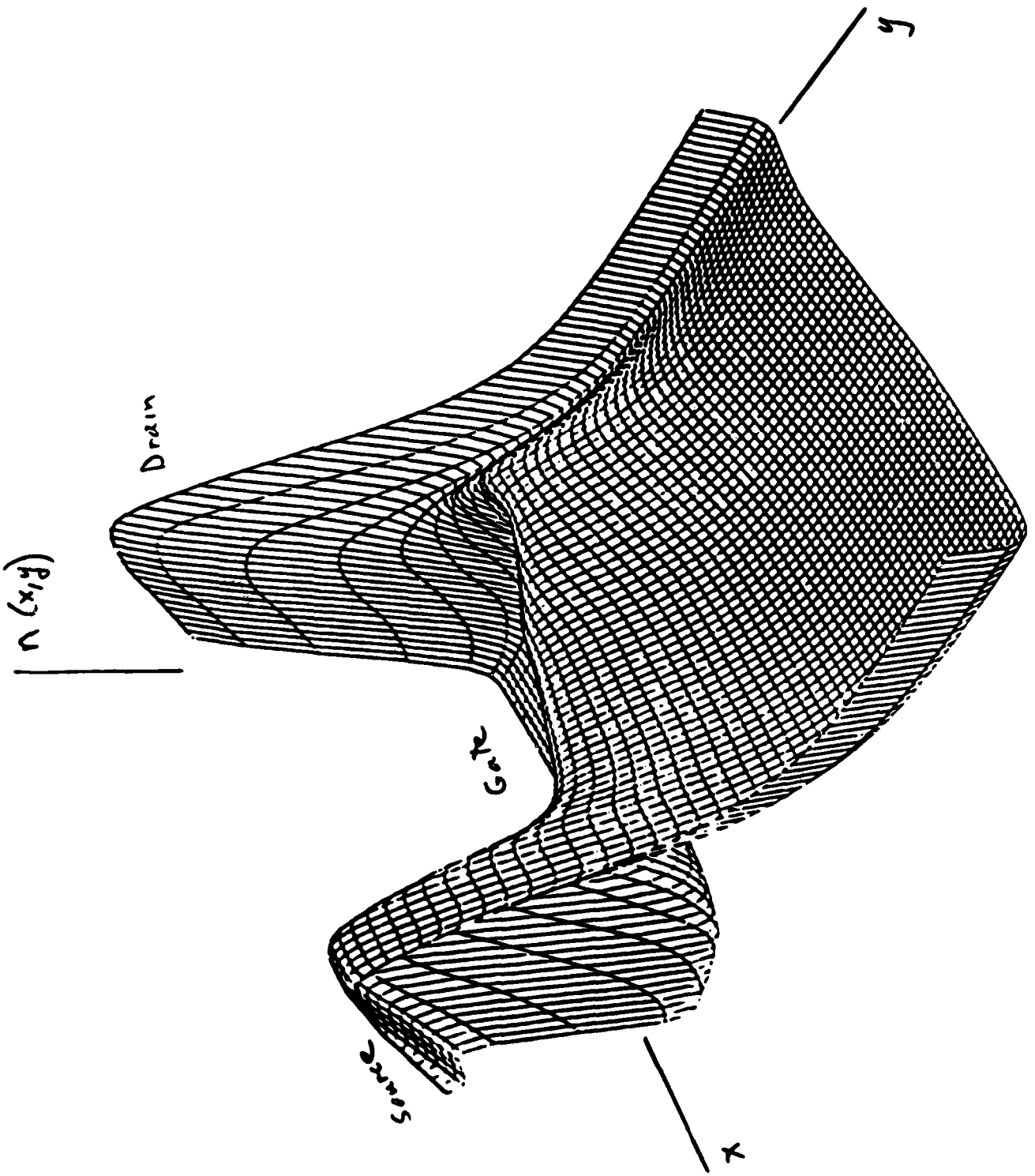


Fig. 10 Electron concentration for a 1 μm gate MESFET with 0.25 μm spacing between the gate and the source/drain contacts at V_{ds} = 2.5 V.

the general discussion above in that both g_m and C_{gd} are increased for the 0.25 μm device. However, there is a net increase in the calculated f_τ of about 4.6%. A calculation at a reduced drain voltage such that the depletion region does not extend to the drain would probably show a larger percentage increase in f_τ.

Table 1

Drain and Source Contacts N = 10^{17} cm^{-3}

V_{DS} = 2.5 V V_{gs} = 0

G-S/Drain Spacing (μm)	g_m (ms)	C_{gd} (fF)	C_{gs} (fF)	f_τ (GHz)
0.5	2.07	4.1	42.0	7.86
0.25	2.2	4.4	42.5	8.22

$$f_\tau = \frac{g_m}{2\pi C_{gs}}$$

6.2 Analytic FET Model Development

The development of the one-dimensional model is nearing completion. The general current expression for describing current flow in MESFET channels with arbitrary doping profiles had previously been developed. This current expression has been used to derive expressions for the device transconductance and gate-source capacitance. The arbitrary doping model has been applied to the constant doping example, and excellent agreement with the results of the flat-profile model was obtained. The drain-souce resistance expression is currently being finalized. The development of this expression will complete the model.

Work on determination of an improved technique for defining the two-piece velocity field characteristic has been completed. This technique uses data obtained from the Monte Carlo transport program to define the low-field

mobility and constant saturated electron velocity. Gate region transit-time is used as the control parameter.

Preliminary investigations of the effects of doping profile variations on device transconductance and gate-source capacitance have been initiated. Ion-implanted profile devices are being compared to flat profile MESFETs. Although various methods for comparing these devices are being considered, the most attractive technique appears to be a comparison of devices with equal values of I_{dss}.

6.3 Monte Carlo Analysis

Modification of the two-dimensional ensemble Monte Carlo analysis to allow simulation of the FET with a doping gradient was completed. Separate doping gradients are included for the channel and contact regions to model the two ion implantation processes. The doping gradients are the same as those used in the 2D device analysis program.

The program was tested on the same device structure previously reported. The operating voltages for the device are V_{gs} = 0 and V_{ds} = 2.5 V. Figures 11 and 12 show the initial net charge density and potential distribution obtained from the 2D device analysis program. After 30 field-adjusting time steps, the net charge density and potential appear to have relaxed to the steady-state solution shown in Figs. 13 and 14. The most noticeable effect on the net charge density is that the accumulation-depletion region near the drain is narrower, more pronounced, and slightly nearer the drain in the Monte Carlo results than is observed for the uniformly-doped device discussed in the last report.

The current density calculated in the above test indicated that a steady-state solution was not reached. The current density was still changing after each time step and the current was not continous across the channel. An estimate of the relaxation time for the current density is the transit time across the channel. For a 2 μm channel device, assuming the average velocity is 2×10^7 cm/s, the transit time is 10 ps. Thus, 200-300 time steps would be

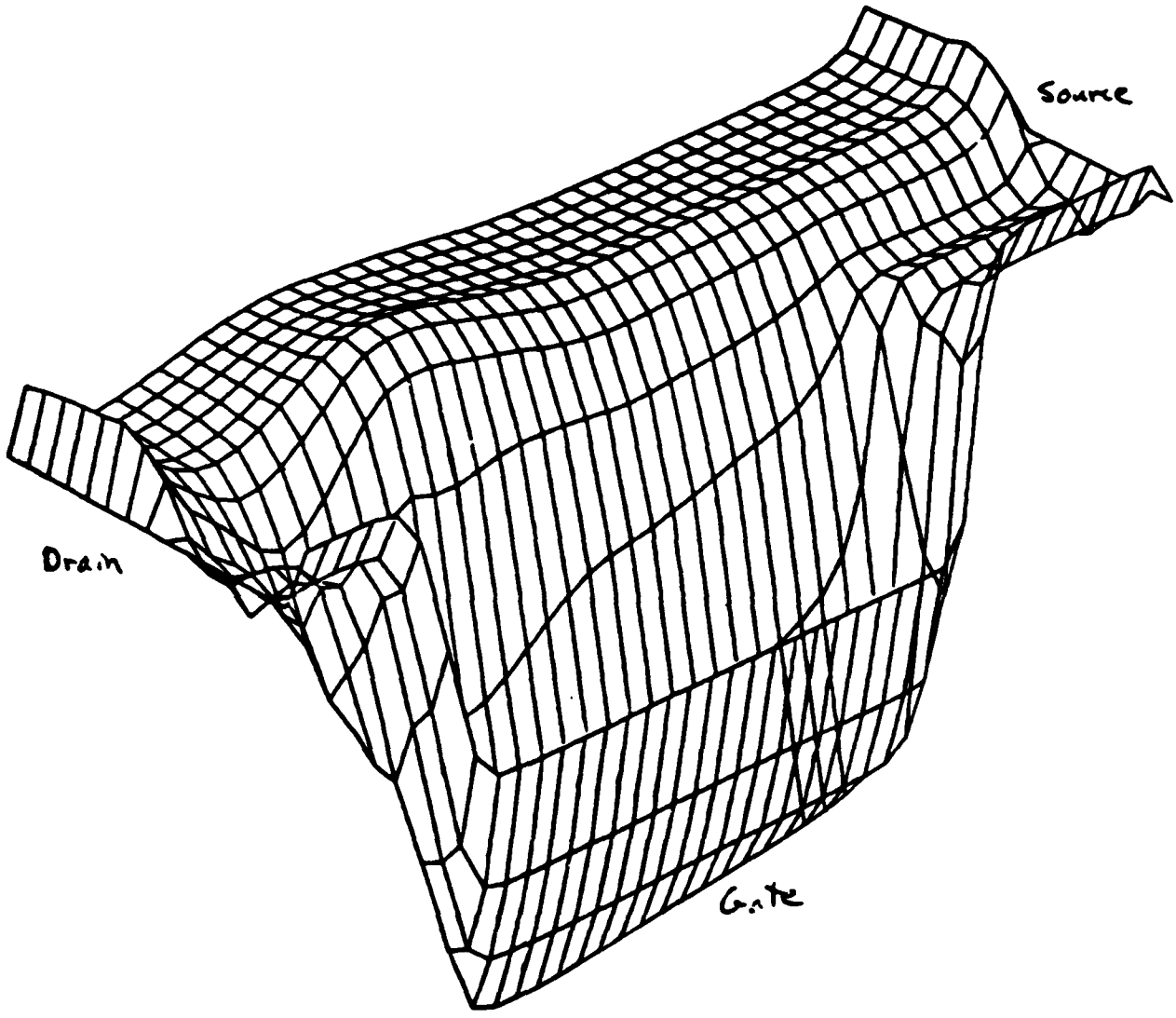


Fig. 11 Initial net charge density for a MESFET device with V_{gs} = 0 and V_{ds} = 2.5 V.

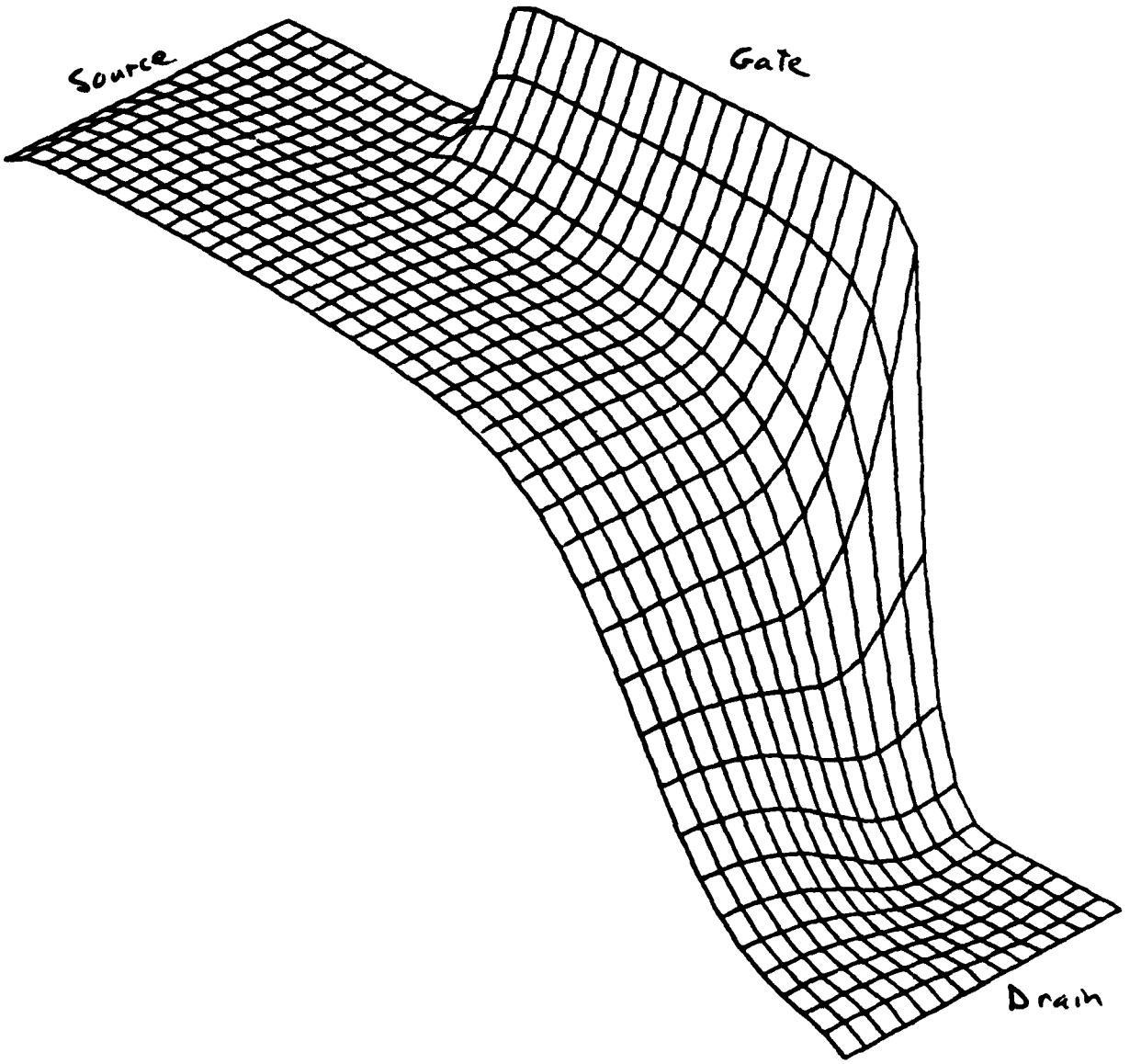


Fig. 12 Initial potential distribution for a MESFET device with V_{ds} = 0 and V_{ds} = 2.5 V.

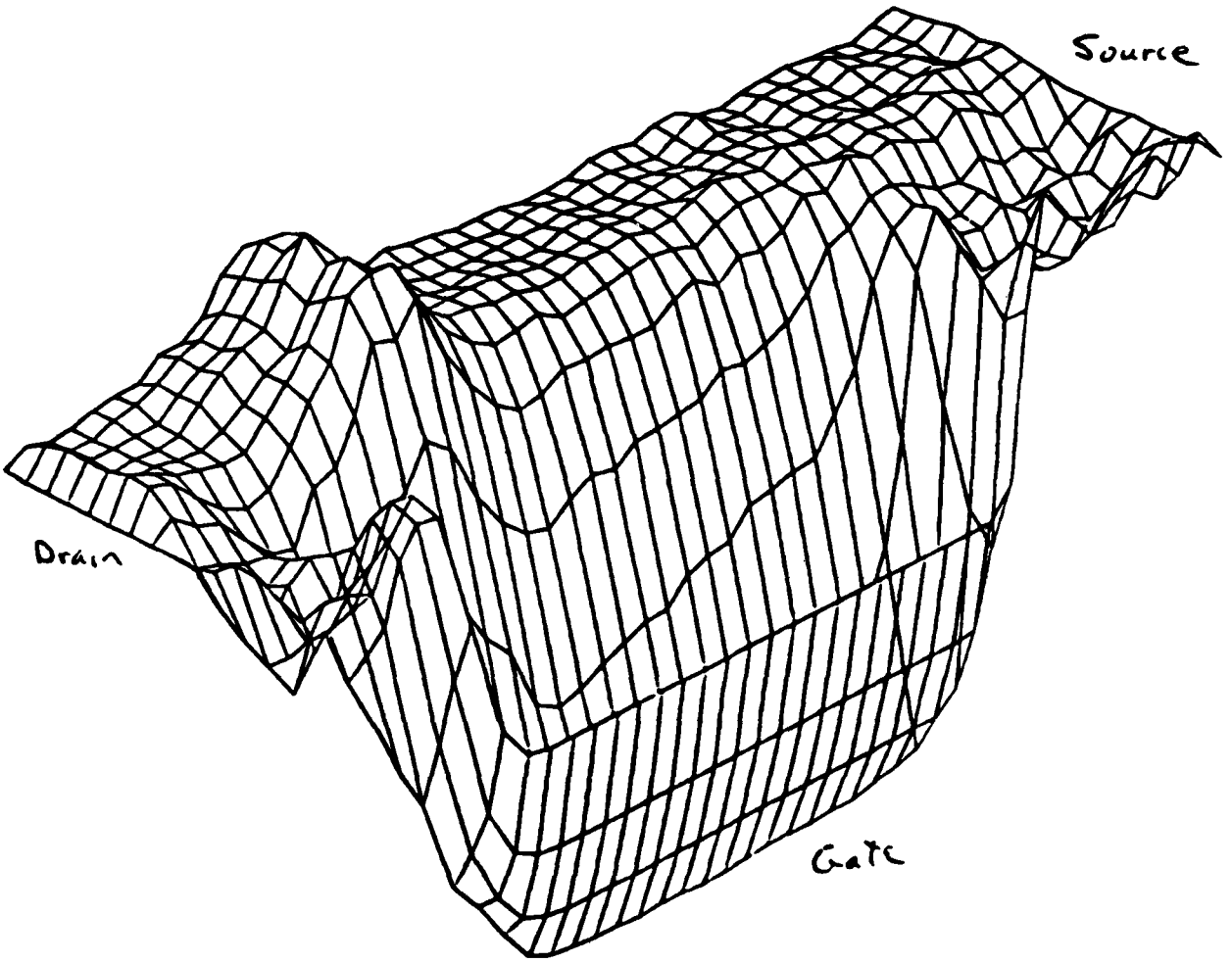


Fig. 13 Net charge density in the MESFET after 30 field-adjusting time steps.

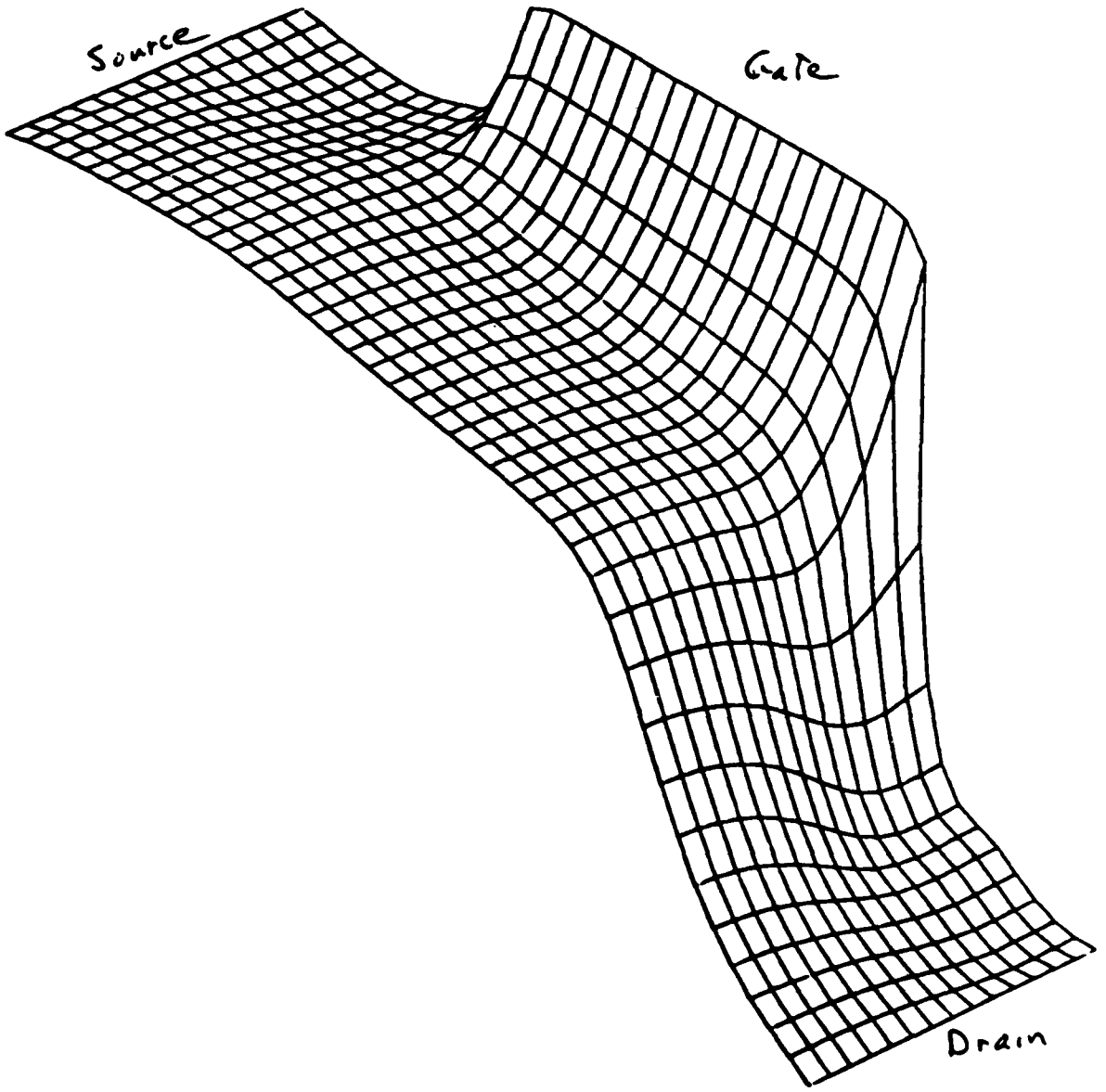


Fig. 14 Potential distribution in the MESFET after 30 field-adjusting time steps.

required to reach a steady state solution for the current density. This may mean that the Monte Carlo method is not an economical method for simulating devices of this size.

Since device analysis programs become less reliable as device dimensions decrease, the 2D Monte Carlo program was tested on a scaled-down device using a 21 × 7 grid. Linear dimensions were scaled by a factor of 1/5, giving a 0.2 μm gate length and a 0.5 μm channel length. The doping concentrations were scaled according to normal scaling laws. The operating voltages were the same as before. The simulation was started from a neutral charge condition instead of using results from the 2D device analysis program. The current density appeared to reach steady state in about 30 time steps. Figure 15 shows the resulting net charge density and potential in the channel of the device. The more noticeable feature in the net charge density is that the accumulation region occurs immediately adjacent to the drain. The current flowing through the channel was calculated to be ~ 36 mA for a channel width of 50 μm.

At the end of the quarter, this program was currently being used to generate the I-V characteristics for the 0.2 μm gate device.

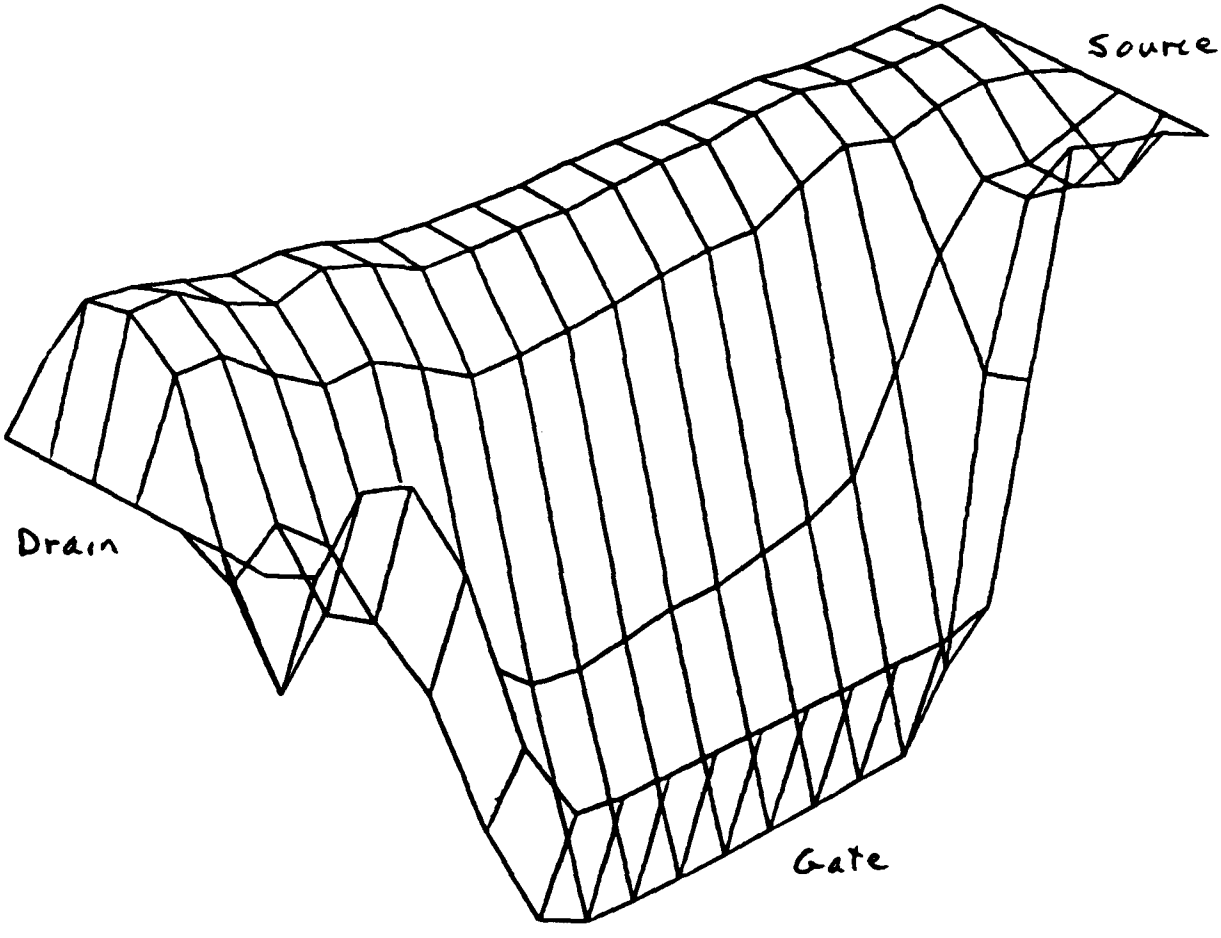


Fig. 15 Net charge density for a scaled down MEFSFET configuration with 0.2 μm gate length and 0.4 μm channel length.

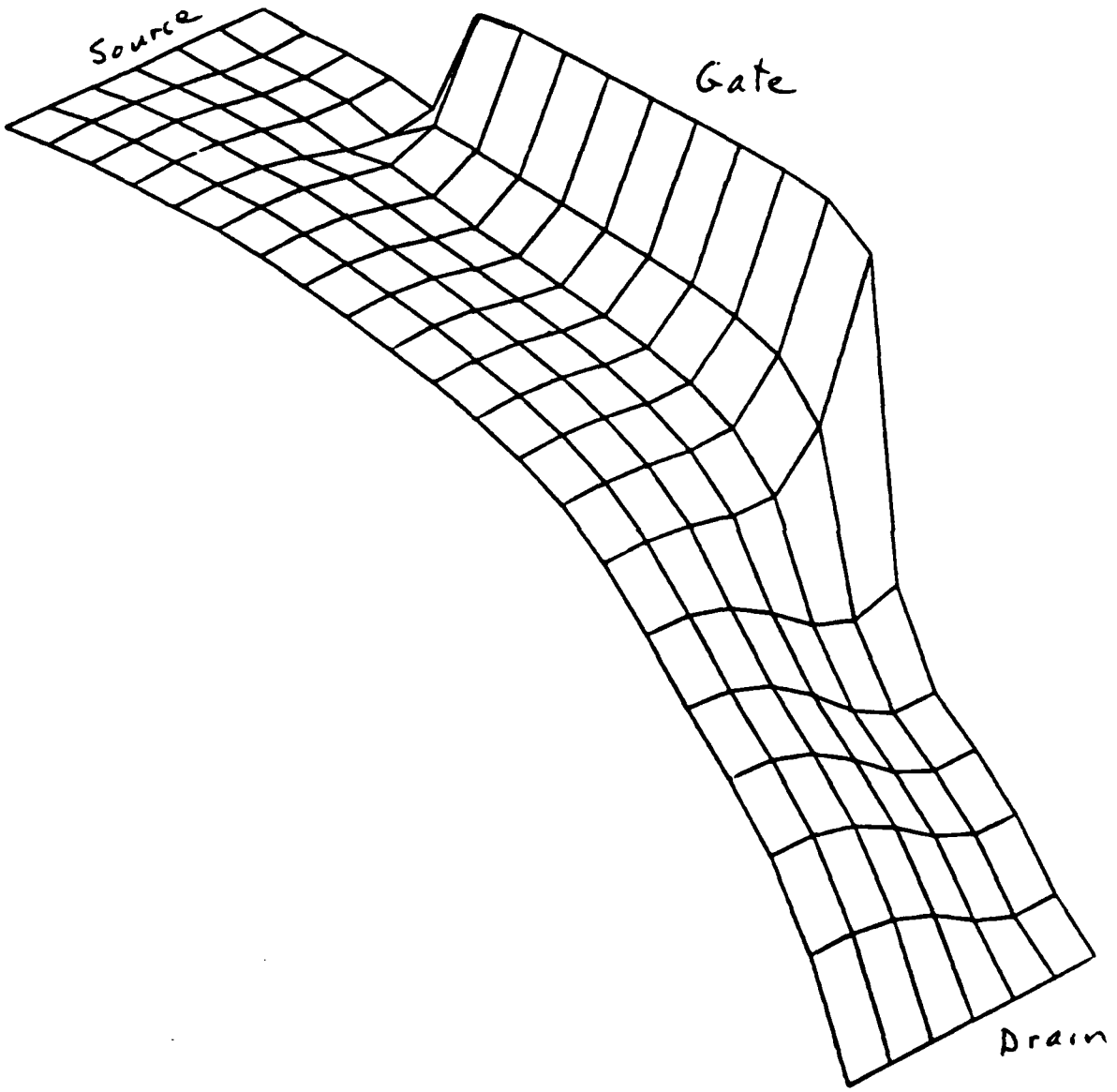


Fig. 16 Potential distribution for a 0.4 μm MESFET configuration.